The GIGAFITTER Project from ongoing R&D to a new track fitter inside CDF

The Gigafitter is a next generation track fitter that has been approved in Italy as an R&D work for future experiments (see document http://www.pi.infn.it/%7Eorso/murst/2005/b_pisa_05.pdf). It is under study during 2007 (Pierluigi Catastini, University of Siena) and if successful it could be used during the final CDF data taking, making SVT much more powerful.

The reduction to virtually zero of the time necessary for the fit is the goal to be achieved with the Gigafitter in order to complete a reconstruction system with high resolution at very high rate.

The device chosen in the R&D as a base for developing the Gigafitter is the Pulsar board. A mezzanine board would house the hardware system implementing the fit algorithm. This R&D configuration allows a very easy application in CDF, if desired.

For the chips to be used for the fit implementation on the mezzanine board, we consider modern FPGAs. Both the Xilinx and Altera companies offer very good devices, for historical reason we prefer Xilinx (Virtex families for examples). In order to allow design of DSP arrays, a single chip of these families contains memories for a total of several Mbytes, and hundreds of 18/25-bits multipliers and adders. The clock runs up to 500 MHz.

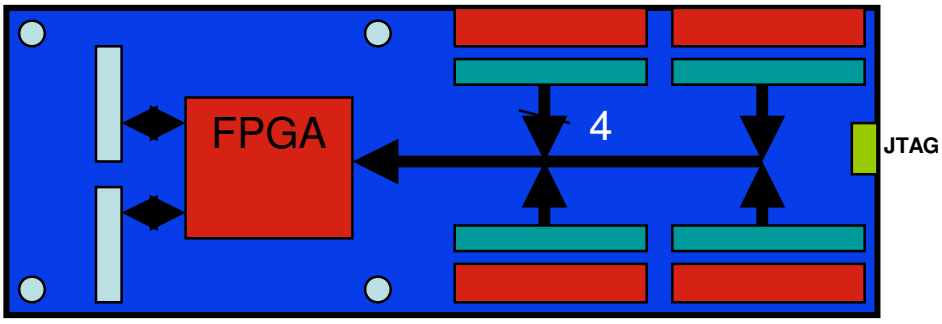
A fit can be executed in a single clock cycle performing all the needed operations in parallel, or even many different fits can be executed in the same clock cycle.

A disadvantage of the TF++ we have now is that the constants require a very large memory because the used multipliers are 8x8 bits and the missing part of the calculation is stored in the memory (one word for each pattern). This feature limits also the usable bank. Having 25x18 bit multipliers allows the use of constant sets that occupy a small memory. We can use many sets of constants and add also patterns crossing mechanical barrels. This means a better SVT efficiency (for a discussion on the SVT efficiency see paragraph 2.1.2 of the CDF Note 6947 and in particular figure 3 showing the effect of cracks between mechanical barrels).

Another clear advantage is the capability to fit many times the same track deleting one particular layer in each different fit. We choose the layer comfiguration producing the best χ^2. The different fits are performed in parallel, without increasing the latency. In the TF++ we have now, a track that has hits in all the layers is fitted using all the 6 points and this fit is preferred even if the χ^2 is bad and the track is lost. It is important at high luminosity to have the possibility to evaluate the fits under the assumption that there is a not negligeble probabilty to have a noisy hit in the combination to be fit. The capability to do many fits and choose the best one reduces the SVT performance degradation due to high detector occupancy.

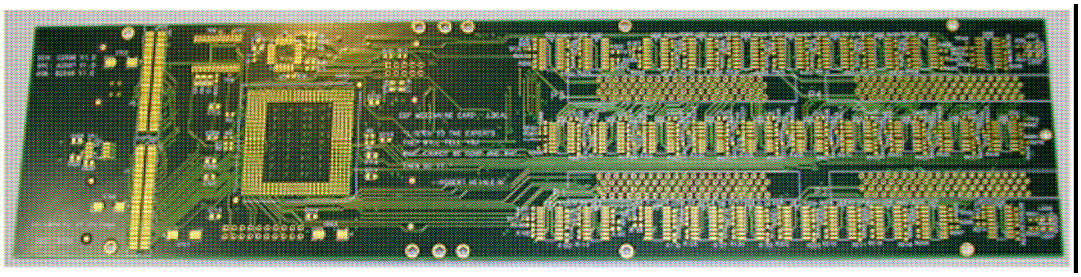
Summarizing, the advantages of the Gigafitter are:

- Velocity: the SVT processing time will improve, how much will be measured directly on data when the R&D will be done.
- Capability to handle AM banks larger than 512 kpatterns (the actual limit comes from TF++). Three important improvements are possible with a larger AM: **A. Lepton coverage** improvement in the forward region; B. The possibility to extend SVT acceptance in **track PT** and **impact parameter**. The extension of SVT coverage in track PT and impact parameter will significantly improve online b-tagging capability, lifetime measurements. Currently SVT reconstructs only tracks with PT> 2 GeV/c and impact parameter smaller than 1.5 mm. We plan to extend these limits: be able to reconstruct tracks down to 1.5 GeV/c in PT and be sensitive for impact parameter up to 2-3 mm. The increase of the muon/electron/tau coverage at CDF for Higgs physics can be achieved coupling high quality tracking provided by SVT in the forward region at LVL2 to high quality LVL2 calorimetric measurements recently provided by the calorimetric upgrade.
- Many sets of constants and better efficiency adding for example intra-barrel patterns(better SVT efficiency).
- Capability to fit each 5/5 road using also any set of 4 hits out of 5 and choose the better result (all the fits can be executed in parallel). This also improves the SVT efficiency and produces more stable performances as a function of luminosity.



For the GigaFitter we plan to exploit the experience gained developing the mezzanine for the Level 2 Calorimeter upgrade. Following a similar design each mezzanine can receive up to 4 Hit Buffer outputs (we plan to substitute the Honda connectors used by the calorimetric processor with the SVT connectors) and the very powerful FPGA on the mezzanine should fit roads from the 4 wedges in parallel. A total of 3 mezzanines will be necessary to handle the 12 wedges. The fitted tracks will be moved to the Pulsar motherboard where they can be corrected for final small non-linearity's effects (large memory will be available in the fourth Pulsar mezzanine), cleaned of ghosts (ghost-buster function) and merged in a single output for the CPU.

The final system will consist of a single Gigafitter Pulsar receiving the 12 wedges, in the case we succeed with the ongoing R&D study to reach such maximum density. In this case the SVT system will be extremely more compact than now, since 12 TF++, 4 final Mergers and 1 Ghost Buster board will be squeezed in a single Pulsar Board. If the achievable logic density is lower, instead of a single Pulsar we will probably need 3 of them.



Here is a photo of the mezzanine already built for the Level-2 calorimeter upgrade, the starting point for the Gigafitter mezzanine. A XC5VSX95T from Virtex5 SXT will replace the old Altera FPGA that is now inside the mezzanine. The new FPGA is able to perform 15 fits in parallel. The Pulsar board in total therefore will be able to perform up to 15 x 3 = 45 fits in parallel, for each SVT input typical clock period of 25 nsec. The Gigafitter is able to do more than a fit/nsec. However the capability to perform at this level is not only due to the computing power of the chip, but also to the I/O capability of the system. Our proposal has enough input bandwidth to saturate the Virtex fitting capabilities. Since the necessary fits will be 6 for each incoming track having 5 silicon hits (1 fit with 5 layers and 5 fits with 4 layers only, to be able to choose the best chi**2 fit between them) the total number of fits required by the 12 wedges providing data in parallel is 72 fits/clock cycle (at high luminosity we expect a large number of 5 hit tracks and a small number of 4/5 hit tracks, since these one will be largely cancelled by the Road Warrior before the Gigafitter).

A scketch of the complete Gigafitter (1 Pulsar with 4 mezzanine boards) is shown in the figure below. It is a very compact solution and not expensive. We have to develop few mezzanines (4 for the experiment + few spares) and use them on a Pulsar that is already available. It is really easy to be tested in parassitic mode at CDF, without causing any problem to the data taking. Man power and support to the project is strong:

1) FPGA firmware: Pierluigi Catastini(ongoing, see talk on webtalk http://www-cdf.fnal.gov/internal/WebTalks/Archive/0704/070418_cdf_italia/04_070418_cdf_italia_Pierluigi_Catastini_1_cdfita_gigafitter.pdf) - University of Siena
2) Mezzanine design, placing and routing - INFN-University of PadovaPulsar firmware (merging function, non-linear effect correction and high memory content mezzanine, ghost-buster function any other useful ideas) - Fermilab team: Laura, Lucas, Virginia?